REMARKS

In the Office Action, the Examiner noted that claims 1-20 are pending in the application. The Examiner rejected claims 1, 2, 6-9 and 13-20, and objected to claims 3-5 and 10-12. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Objections

The Examiner has objected to dependent claims 3-5 and 10-12 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. The Applicant thanks the Examiner for indicating allowable subject matter, but believe independent claims 1 and 8, from which these dependent claims depend, are allowable over the prior art of record for the reasons set forth below. Thus, the Applicant contends that claims 3-5 and 10-12 should distinguish over the prior art of record, since each claim depends from independent claims 1 or 8. Therefore, the Applicant respectfully requests that the objection to claims 3-5 and 10-12 be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1, 2, 6-9 and 13-20 as being anticipated by Rahut (United States patent 6,766,504, issued July 20, 2004). The rejection is respectfully traversed.

More specifically, the Examiner stated that Rahut teaches a router and timing engine for placing and routing a circuit design based on template connections and for analyzing the circuit design using timing parameters. (Office Action, p. 2). The Examiner stated that Rahut "clearly suggest[s] that the timing information includes sets of timing attributes for one or more interconnects in each logic level of routing topology, where each set of the timing attributes [is] associated with one of a plurality of locations within the IC in which the circuit is placeable." (Office Action, p. 3). The

Examiner concluded that Rahut anticipates Applicant's invention recited in claims 1-2, 6-9, and 13-20.

Rahut generally teaches a routing technique for integrated circuits. In particular, the routing process begins with a network having resources (circuit elements) and connections (a segment connecting two resources). (Rahut, col. 4, lines 9-21; col. 8, lines 30-43). That is, in Rahut, the resources have already been placed. The connections are then routed in a resource mode and timing information of the network is updated. (Rahut, col. 8, lines 44-59). Critical connections are identified and sorted by logic level. (Rahut, col. 8, line 60 through col. 9, line 8). Critical connections from a logic level identified in accordance with a heuristic are routed in a delay mode. (Rahut, col. 9, lines 9-24).

Rahut, however, does not teach each and every element of Applicant's invention recited in claim 1. Namely, Rahut does not teach or suggest determining sets of timing attributes for a routing topology of a template, where each set of timing attributes is associated with one of a plurality of locations within an integrated circuit in which the circuit design is placeable. While Rahut generally describes timing information (e.g., minimum path slack and number of critical paths), Rahut does not teach or suggest determining multiple sets of such attributes respectively associated with multiple placements of the design in an integrated circuit. Rahut is not concerned with and does not disclose placement of a circuit design. Rather, Rahut discloses a routing technique, where it is assumed the design has already been placed (i.e., the resources have been placed such that they are connectable). There is no disclosure in Rahut of determining timing attributes for multiple placements of a circuit design.

The Examiner indicated that Rahut "suggests" that timing information includes sets of timing attributes associated with locations in an IC in which the circuit design is placeable. However, "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Thus, a mere suggestion is not sufficient for an anticipation rejection. Since Rahut does not teach determining sets of timing attributes for respective placements of a circuit design in an integrated circuit, Rahut does not

teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Rahut does not anticipate Applicant's invention recited in claim 1.

Independent claims 8, 15, 17, and 19 include features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Rahut does not anticipate the invention of claims 8, 15, 17, and 19. Finally, claims 2, 6-7, 9, 13-14, 16, 18, and 20 depend, either directly or indirectly, from claims 1, 8, 15, 17, and 19 and recite additional features therefor. Since Rahut does not anticipate Applicants' invention as recited in claims 1, 8, 15, 17, and 19, dependent claims 2, 6-7, 9, 13-14, 16, 18, and 20 are also not anticipated and are allowable. Therefore, the Applicant contends that claims 1, 2, 6-9 and 13-20 are not anticipated by Rahut and, as such, fully satisfy the requirements of 35 U.S.C. §102. The Applicant respectfully requests that the objection to such claims be withdrawn.

CONCLUSION

Thus, the Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Kim Kanzaki at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 12, 2006.

Pat Tompkins
Name

Signature